PATENT ABSTRACTS OF JAPAN

(11) Publication number: 10041482 A

(43) Date of publication of application: 13.02.98

(51) Int: CI

H01L 27/108 H01L 21/8242 H01L 21/285 H01L 21/768

(21) Application number: 08189424

(22) Date of filing: 18.07.96

(71) Applicant:

FUJITSU LTD

(72) Inventor:

IKEMASU SHINICHIROU

OKAWA SHIGEMI

(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57) Abstract:

PROBLEM TO BE SOLVED: To enable a nitride film spacer SAC structure to be applied to a polyside structure so as to enhance a semiconductor device in degree of integration by a method wherein a second insulating film of silicon nitride is formed covering a first insulating film formed on the upside and side wall of a conductive layer pattern.

SOLUTION: A gate electrode of laminated structure composed of a silicon film 4 and a silicide film 5 is formed on a substrate 1 possessed of an active layer region demarcated with a field insulating film 2 through the intermediary of a gate oxide film 3. The upside and side face of the gate electrode are covered with a silicon nitride film 8. An oxide film 6 is provided between the silicon nitride film 8 serving as a spacer and the side wall of the gate electrode. The above structure can be applied to another wiring layer such as a bit line of polycide structure or the like besides the gate electrode of a MOS transistor. By this setup, an oxide film can be formed through a thermal oxidation method. A silicide film can be restrained from being

separated off by the use of the above oxide film.

COPYRIGHT: (C)1998,JPO

